E-mode Planar L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFETs with $InP/Al_2O_3/HfO_2$ (EOT = 0.8 nm) Composite Insulator

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Abstract

We have successfully demonstrated a three-step recess process to fabricate high performance E-mode planar InGaAs MOSFETs. Our devices feature a composite gate insulator with $InP/Al_2O_3/HfO_2$. An L_g=35 nm InGaAs MOSFET with EOT = ~ 0.8 nm exhibits V_T = 0.17 V, R_{ON} = 285 Ohm-μm, DIBL = 135 mV/V and S = 115 mV/dec, as well as a negligible dispersion and hysteresis behavior. Most importantly, our device displays the highest value of g_{m_max} > 2 mS/μm at V_{DS} = 0.5 V in any III-V MOSFETs.

Introduction

The outstanding carrier transport properties of III-V compound semiconductors have fueled interest on these materials for use in the channel material of a future scaled CMOS technology [1-9]. Particularly, indium-rich $In_xGa_{1-x}As$ (x > 0.53) materials are endowed with very high electron mobility ($\mu_{n,eff}$) and virtual-source-injection velocity (v_{ox}). Not only are both quantities directly related to the FET theory and carrier transport properties, but also unique device FOM that ultimately determines the drain current density (I_{ON}) and the transistor switching speed (CV/I).

In this paper, we propose a three-step recess process that allows us to fabricate high performance enhancement-mode (E-mode) planar InGaAs MOSFETs with $InP/Al_2O_3/HfO_2$ composite insulator. Our long- and short-channel MOSFETs with EOT = ~ 0.8 nm exhibits excellent carrier transport properties and logic characteristics.

Experimental

Fig. 1 shows a cross section of the device. From top to bottom, the epitaxial layer structure consists of a heavily doped multi-layer cap ($In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, InP, $In_{0.52}Al_{0.48}As$), 1-nm InP insulator, 10-nm $In_{0.7}Ga_{0.3}As$ channel, 5-nm $In_{0.52}Al_{0.48}As$ spacer, inverted Si δ-doping and 300-nm $In_{0.52}Al_{0.48}As$ barrier on InP substrate. We have optimized a growth temperature and inverted Si δ-doping density which led to the electron Hall mobility ($\mu_{n,hall}$) close to 8,500 cm^2/V-sec with $n_s = 1 \times 10^{12}$ /cm^2 at 300 K. **Fig. 1**, shows conduction-band (E_C) and carrier concentration (n_s) profile at S/D access region. Black-colored lines are with n+ $In_{0.53}Ga_{0.47}As$ cap, whereas blue-colored ones with n+ $In_{0.52}Al_{0.48}As$ cap. Not only does a use of heavily doped $In_{0.52}Al_{0.48}As$ cap lower a potential barrier through both InP layers in the S/D access region, but it also significantly increases the electron concentration in the channel. Both are very effective in reducing R_S and R_D.

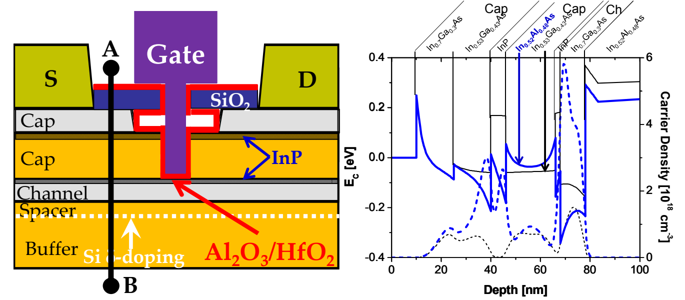

Fig. 1 (Left) Schematic of recessed planar InGaAs Quantum-Well (QW) MOSFETs with $InP/Al_2O_3/HfO_2$, and (b) (Right) 1D simulation at S/D access region (A-to-B).

Fig. 2 highlights a proposed three-step gate process in this work. After S/D ohmic contact with 2 μm spacing, a fine gate pattern using single-layer ZEP-520A is defined by e-beam lithography. This is transferred to a passivating SiO_2 layer by CF_4 plasma (a). Following this, InGaAs cap is etched isotropically using a mixture of citric acid and H_2O_2, and the InP cap and part of the InAlAs cap are etched anisotropically by a low-damage Ar-plasma (b). Remaining $In_{0.52}Al_{0.48}As$ cap is fully etched by using a diluted citric acid solution (c). Immediately after removing the ZEP520A, Al_2O_3/HfO_2 (0.5/1.5 nm) is sequentially deposited at 250 °C by ALD (d). Finally, a gate metal stack of Pd/Ti/Au is formed. **Fig. 3** show a SEM image after three-step recess, and a TEM image for the cross section of a 35-nm device. In addition to the e-beam defined narrow gates, we have made optical gate patterns from 4 μm to 1 μm, to investigate a carrier transport property.

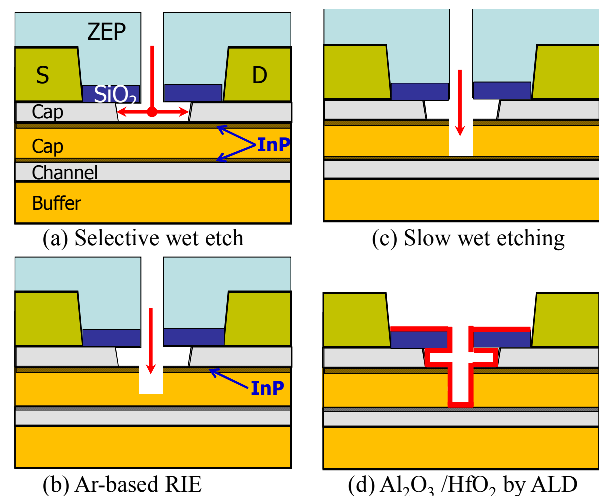

Fig. 2 Sketch of proposed three step gate recess process.

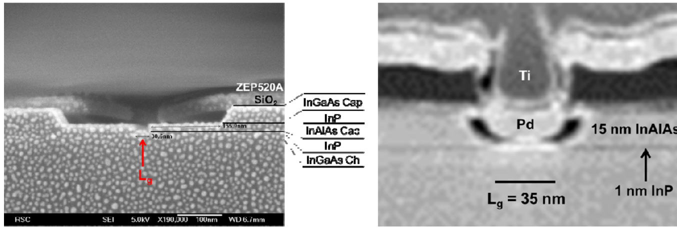

Fig. 3 (Left) SEM image after three-step-recess. This corresponds to the step (c) in Fig. 2. Final opening by slow wet etching for n+ InAlAs cap determines the physical gate length (L_g). (Right) TEM image for L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFETs with $InP/Al_2O_3/HfO_2$ composite insulator. Gate metal is made out of Pd/Ti/Au stack.

Results and discussion

A. *Long-channel InGaAs MOSFETs*

Fig. 4 shows subthreshold and gate leakage current (I_G) of L_g = 2 µm (optical) devices with Mo/Ti/Pt/Au gate metal stack for two types of gate insulators, such as HfO_2 (black) and Al_2O_3/HfO_2 (red). Using ~ 0.5 nm Al_2O_3 as an ICL (Interface-Control-Layer) [6] leads to a far better interface quality on MBE-grown 1-nm InP, clearly manifested in the subthreshold behavior, such as DIBL = 40 mV/V. We have carried out a pulsed I-V measurement, to evaluate the dielectric-to-channel interface quality, as shown in **Fig. 5**. Pulse width is 200 ns, and operating condition (bias point) is V_{GS} = - 0.8 V and V_{DS} = 1 V in dynamic I-V measurement. Consistent with subthreshold characteristics, the device with composite Al_2O_3/HfO_2 insulator exhibits almost a dispersion-free behavior, in comparison to one with HfO_2 insulator.

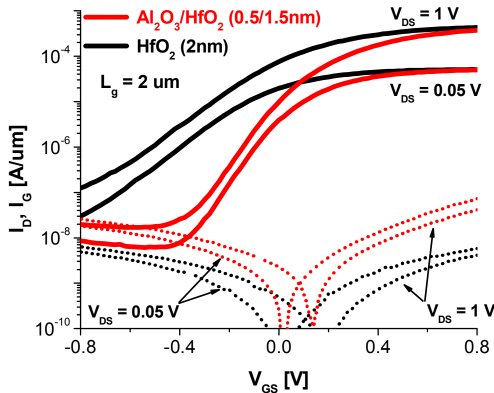

Fig. 4 Subthreshold and gate leakage (I_G) characteristics of L_g = 2 µm devices with Mo/Ti/Pt/Au metal gate on HfO_2 (black) and Al_2O_3/HfO_2 (red) insulator, at V_{DS} = 0.05 V and 1 V.

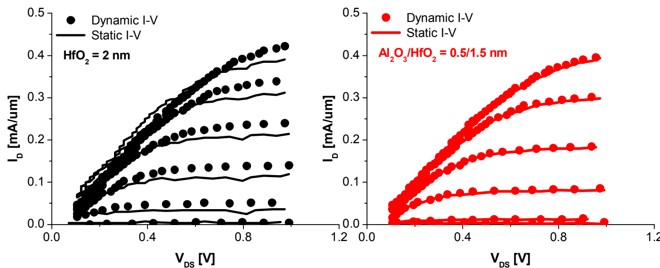

Fig. 5 Pulsed I-V characteristics using a DIVA instrument for L_g = 2 µm (optical) $In_{0.7}Ga_{0.3}As$ MOSFETs, such as HfO_2 (black, on the left) and Al_2O_3/HfO_2 (red, on the right).

Fig. 6 shows transconductance (g_m) characteristics of the devices with Al_2O_3/HfO_2 composite insulator at V_{DS} = 1 V, for various values of L_g. Note that the device with L_g = 2 µm already exhibit g_{m_max} > 0.6 mS/µm and one with L_g = 1.2 µm g_{m_max} > 0.8 mS/µm, which are the highest values in any III-V MOSFET at those L_g dimensions.

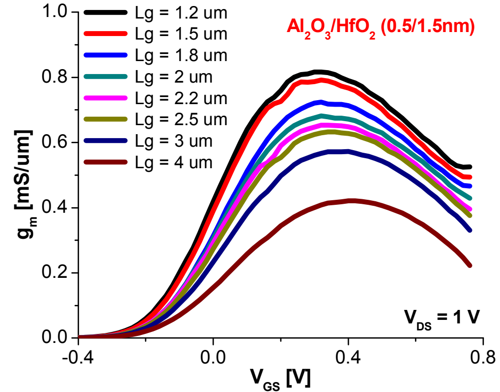

Fig. 6 Transconductance (g_m) characteristics of various L_g (optical) devices with Mo/Ti/Pt/Au metal gate on Al_2O_3/HfO_2 insulator at V_{DS} = 1 V.

In trying to understand such performance, we have carried out a carrier transport analysis in the sense of '*effective*' mobility (μ_{eff}), somewhat similar to [10]. At V_{DS} = ~ 0 V, we first measured high-frequency small-signal S-parameters up to 50 GHz, and then performed a small-signal modeling to extract total gate capacitance ($C_{g,total} = C_{gs} + C_{gd}$, **Fig. 7**) and intrinsic output conductance (g_{oi}) for various different values of L_g, with R_S and R_D removed. The intrinsic gate capacitance (C_{gi}) and intrinsic charge (Q_{gi}) are extracted by using the same procedure in [10], and were plotted in the inset of **Fig. 7**. Finally, μ_{eff} was computed based on Q_{gi} and g_{oi}, and plotted in **Fig. 8**. Interestingly, the mobility flattens out for low n_s. This is an area where the traditional technique fails because of D_{it} contamination, whereas the proposed technique doesn't suffer from because both capacitance and conductance are extracted from high-frequency S-parameters. At $n_s = 2 \times 10^{12}$ /cm^2, a long channel device exhibits μ_{eff} in excess of 7,000 cm^2/V-s.

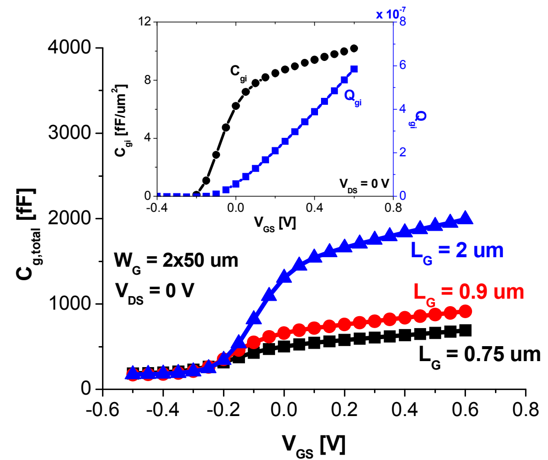

Fig. 7 Extracted $C_{g,total}$ (=$C_{gs} + C_{gd}$) vs. V_{GS} at V_{DS} = 0 V. Inset is the extracted intrinsic gate capacitance (C_{gi}) and corresponding intrinsic gate charge (Q_{gi}), as in [10].

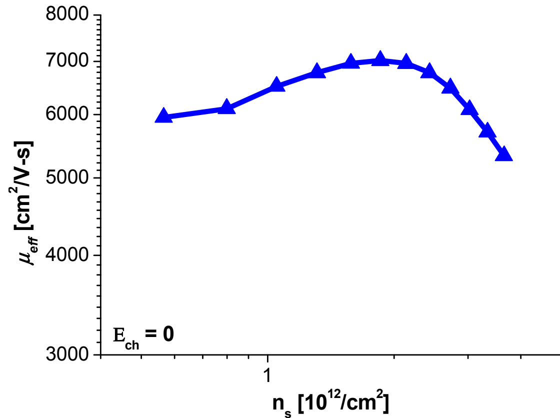

Fig. 8 Extracted effective mobility (μ_{eff}) against n_s.

B. *Short-channel InGaAs MOSFETs*

Fig. 9 shows typical output characteristics of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au metal gate on composite Al_2O_3/HfO_2 insulator. Particularly, Pd was chosen for E-mode operations due to its higher work-function. The device exhibits excellent pinch-off and saturation behavior up to V_{DS} = 0.5 V. A fairly low value of R_{ON} = 285 Ω-μm is obtained. **Fig. 10** shows subthreshold and transfer characteristics of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au metal gate on composite Al_2O_3/HfO_2 insulator. Using a criteria of I_D = 1 μA/μm, the device shows as follows; V_T = +0.17 V (E-mode), S = 115 mV/dec and DIBL = 135 mV/V. Besides, our device exhibits very little hysteresis behavior of less than 10 mV.

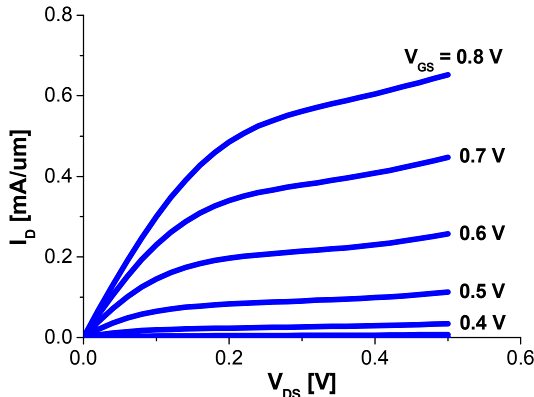

Fig. 9 Output characteristics of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au on composite Al_2O_3/HfO_2 insulator.

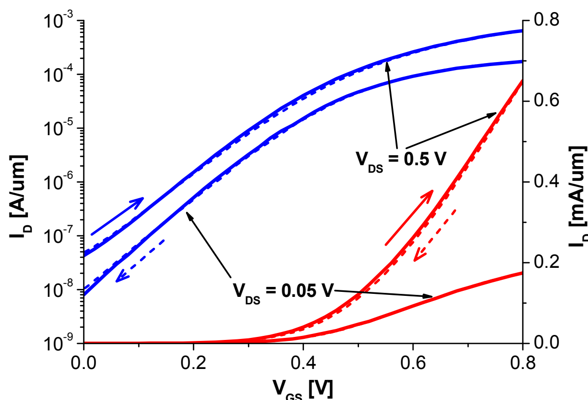

Fig. 10 Subthreshold and transfer characteristics of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au metal gate on composite Al_2O_3/HfO_2 insulator.

Fig. 11 shows g_m of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au metal gate on composite Al_2O_3/HfO_2 insulator. Maximum transconductance (g_{m_max}) is 2.1 mS/μm at V_{DS} = 0.5 V, the highest ever reported in any III-V MOSFETs. Inset is the gate leakage current, where I_G is lower than 10 nA/μm for all the measured bias conditions.

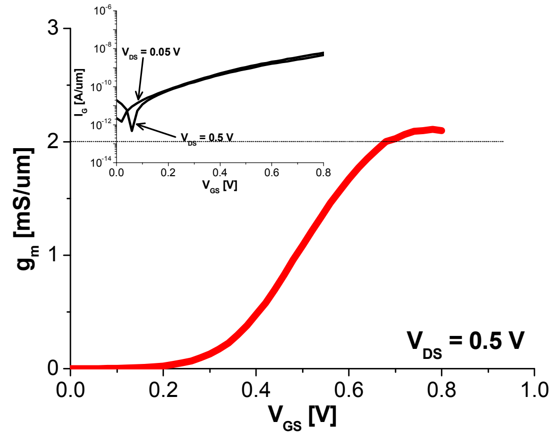

Fig. 11 Transconductance (g_m) characteristics of L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Pd/Ti/Au metal gate on composite Al_2O_3/HfO_2 insulator, at V_{DS} = 0.5 V.

C. *Benchmarking and Discussion*

In order to assess the significance of our work, we have benchmarked our devices against reported III-V MOSFETs. **Fig. 12** compares g_{m_max} versus L_g of our recessed $In_{0.7}Ga_{0.3}As$ MOSFETs to prior reports on III-V MOSFETs in the literature. Clearly, the devices in this work exhibit the highest g_{m_max} from long channel to sub-100 nm regime of all the III-V MOSFETs. **Fig. 13** compares Q-factor of our recessed $In_{0.7}Ga_{0.3}As$ MOSFETs with composite Al_2O_3/HfO_2 insulator to other reports, as proposed in [11].The result in this work indicates Q = ~ 20, which is the highest in any III-V MOSFET. **Fig. 14** plots virtual-source injection velocity (v_{x0}) against DIBL for InGaAs MOSFETs at V_{ds} = 0.5 V, together with those of III-V HFETs and Si nFETs [10]. As in [10], v_{x0} increases as DIBL increases. At V_{ds} = 0.5 V and DIBL = 100 mV/V, v_{x0} in our InGaAs MOSFETs is about 6× higher than that of state-of-the-art strained Si MOSFETs.

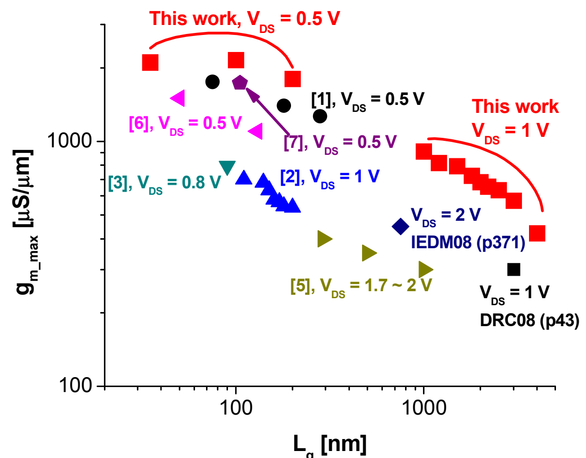

Fig. 12 Maximum transconductance (g_{m_max}) against of L_g, including other reports on III-V MOSFETs in the literature.

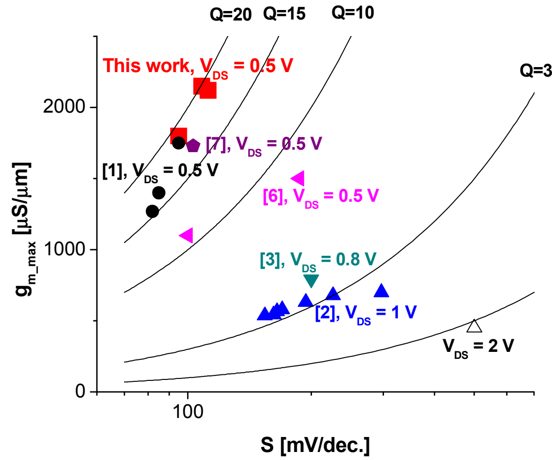

Fig. 13 Maximum transconductance (g_{m_max}) as a function of subthreshold-swing (S), including reports in the literature.

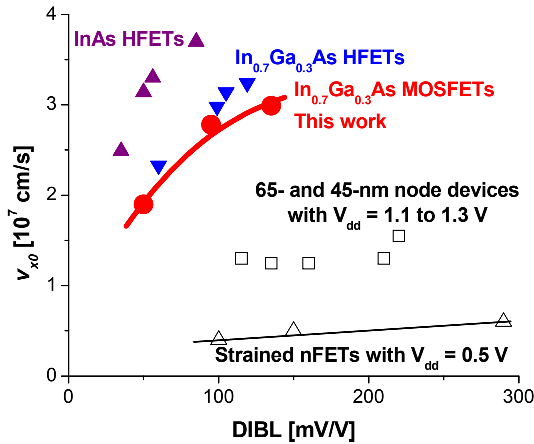

Fig. 14 Extracted virtual-source-injection velocity (v_{x0}) vs. DIBL for $In_{0.7}Ga_{0.3}As$ MOSFETs at V_{dd} = 0.5 V, together with those of 65- and 45-nm nFETs and advanced Si nFETs at V_{dd} = 0.5 V, and advanced III-V HFETs at V_{dd} = 0.5 V [10].

A striking aspect of our $In_{0.7}Ga_{0.3}As$ MOSFETs with composite insulator ($InP/Al_2O_3/HfO_2$ = 1/0.5/1.5 nm) is their outstanding g_m down to L_g = 35 nm with excellent subthreshold characteristics. This is mainly thanks to the proposed three-step-recess process plus the design of the novel capping structures, together with aggressive EOT scaling (EOT = ~ 0.8 nm). Finally, **Fig. 15** summarizes the analysis on R_{ON}. With further device optimization in the form of a self-aligned gate design and a tight control for L_{side}, the proposed III-V MOSFETs in this work could be the technology of choice for future applications.

Summary

We have demonstrated E-mode planar L_g = 35 nm InGaAs MOSFET with composite $InP/Al_2O_3/HfO_2$ insulator, based on three-step recess process. L_g = 35 nm devices exhibit excellent transport and logic characteristics at V_{DS} = 0.5 V, such as g_{m_max} = 2.1 mS/μm, R_{ON} = 285 Ω-μm. DIBL = 135 mV/V and S = 115 mV/dec. Most importantly, our device exhibits the highest value of g_{m_max} in any III-V MOSFETs from long channel to sub-100 nm regime. In addition, we have carried out a carrier transport analysis, indicating μ_{eff} > 7,000 cm^2/V-s at $n_s = 2 \times 10^{12}$ /cm^2 at room temperature.

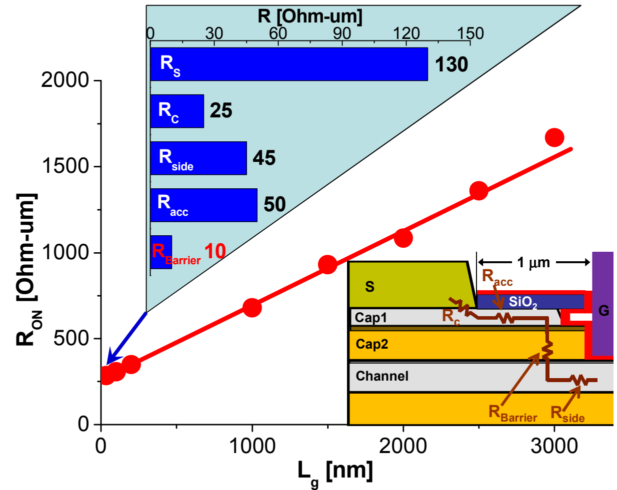

Fig. 15 On-resistance (R_{ON}) as a function of L_g for $In_{0.7}Ga_{0.3}As$ MOSFETs in this work. Inset is a sketch that describes each portion of source-resistance (R_s), such as R_c, R_{acc}, $R_{Barrier}$ and R_{side}. Upper inset highlights extracted values for each component in R_s.

Acknowledgment

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